24.2: Self-Biased, High-Bandwidth, Low-Jitter 1-to-4096 Multiplier Clock Generator PLL

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Clock Generator PLLs for ASICs

- Most ASICs PLLs for clock generation, but …
  - Use different frequencies and multiplication
Optimal PLL Design

- For each $F_{\text{OUT}}$ and $N$, one must adjust loop parameters for both minimum jitter and stability.

- For clock generators (track input clocks)
  \[ \omega_{\text{REF}} = 2\pi \cdot \frac{F_{\text{OUT}}}{N} \]
  - Loop bandwidth : $\omega_N \sim \omega_{\text{REF}}/20$
  - Damping factor : $\zeta \sim 1$
  - Third-order pole : $\omega_C \sim \omega_{\text{REF}}/2$

- Circuit parameters (e.g. $I_{\text{CH}}$, $R$) must vary with $F_{\text{OUT}}$ and $N$!
Addressing Diverse Specifications

- Designing a different PLL for each ASIC
  - Easier to meet the specification, but …
  - Verifying all designs is difficult and costly

- Our Goal: One PLL design for all ASICs
  - Only one design needs verification, but …
  - Loop parameters must adjust automatically to satisfy wide range of $F_{OUT}$ and N
Challenges

- Self-biased PLLs [Maneatis ‘96] adjust for $F_{OUT}$
  - Achieve fixed $\omega_N/\omega_{REF}$ and $\zeta$ indep. of PVT

- But, Self-Biased PLLs do NOT adjust for $N$
  - $\omega_N/\omega_{REF}$ and $\zeta$ vary with $N$ (want fixed)
  - $\omega_C/\omega_{REF}$ varies with $N$ (want fixed)

- This talk extends Self-Biased PLLs for wide ranges of $N$ with a new loop filter network
Outline

- Introduction
- Review of Self-Biased PLLs
- Pattern Jitter Issues
- Loop Filter Architecture
- Implementation of Key Circuits
- Measured Results
- Conclusions
Second-Order PLLs

\[
P_O(s) = \frac{1 + 2 \cdot \zeta \cdot (s / \omega_N)}{1 + 2 \cdot \zeta \cdot (s / \omega_N) + (s / \omega_N)^2}
\]

\[
\omega_N = \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot \frac{1}{C_1}}
\]

\[
\zeta = \frac{1}{2} \cdot \omega_N \cdot R \cdot C_1
\]
Self-Biased PLLs

\[ R = \frac{1}{g_m}, \quad I_{CH} = x \cdot I_D, \quad F_{VCO} = g_m / C_B \]
Self-Biased PLLs

- With Self-Biased PLLs

\[ \frac{\omega_N}{\omega_{\text{REF}}} = \frac{1}{2\pi} \cdot \sqrt{x \cdot N} \cdot \sqrt{C_B/C_1} \sim \sqrt{x \cdot N} \]

\[ \zeta = \frac{1}{4} \cdot \sqrt{x/N} \cdot \sqrt{C_1/C_B} \sim \sqrt{x/N} \]

- \( \frac{\omega_N}{\omega_{\text{REF}}} \) and \( \zeta \) are constant with \( F_{\text{OUT}} \), BUT not with \( N \)
Pattern Jitter / Spurious Noise

- Phase corrections every rising reference edge can cause disruptions to nearby output cycles
  - Periodic noise pattern repeats every ref. cycle or N output cycles

\[\text{CK}_{\text{REF}} \quad \text{CK}_{\text{OUT}} \quad \text{V}_{\text{CTL}} \quad \text{SHORT}\]

- Typical causes
  - Charge pump imbalances or leakage
  - Jitter in reference clock (aperiodic result)
Shunt Capacitor

- Use third-order pole to extend disturbance with reduced amplitude over many output cycles

- Problem with varying N using fixed capacitor
  - Extended number of cycles NOT function of N
  - Too few for large N → Pattern jitter
  - Too many for small N → Instability
Proposed Loop Filter

- Use switched capacitor filter network to
  - Output scaled amplitude error signal with N output cycle duration [Maxim ’01]

Want a simple solution using this approach that is compatible with Self-Biased PLLs
Original Filter Network

- Only need to filter feed-forward path
Sampled Feed-Forward Network

- Sample phase error and generate proportional current that is held constant for $N \cdot T_{\text{OUT}}$
- Sampled error is reset at end of ref. cycle
  - Need $V_{\text{RST}} = V_{\text{CTL}}$ as zero bias level
Complete Filter Network

- Reset $C_2$ to $V_{CTL}$ directly
  - Eliminates $C_1$ charge pump
- Equivalent feed-forward control gain
  $Q_O \sim N \cdot Q_I$
Loop Dynamics

- With this new loop filter network we achieve
  \[ \frac{\omega_N}{\omega_{REF}} \sim \sqrt{x \cdot N} \quad \zeta \sim \left(\frac{Q_O}{Q_I}\right) \cdot \sqrt{x/N} \sim \sqrt{x \cdot N} \]

- Need to keep \( \omega_N/\omega_{REF} \) and \( \zeta \) constant with \( N \)
  - Just scale charge pump current with \( 1/N \) (=x)

- More detailed analysis will show
  \[ \frac{\omega_N}{\omega_{REF}} = \frac{1}{2\pi} \cdot \sqrt{C_B/C_1} \]
  \[ \zeta = \frac{1}{4} \cdot \sqrt{C_B \cdot C_1/C_2} \]

- Both are independent of \( F_{OUT} \), \( N \), and PVT!
Complete Self-Biased CGPLL
Self-Biased Filter Network
Filter Network Reset Switches

- Can switch to $V_{CTL}$ independent of voltage level
Inverse-Linear Current Mirror

- Need to generate $I_{CH} = I_D / N$
- Use switches to adjust device size on input side
  - For $N=1$~4096, need 12 binary weighted legs
  - Need size range of 2048:1 → Too much area!
Multi-Stage Linear CM

- Solution to size problem with LINEAR control
  - Use multiple device groups operating at different but ratioed current densities
  - Can have large ranges using small devices
Multi-Stage Inverse-Linear CM

- Just diode connect multi-stage linear current source and use as input side of current mirror
- Can output gate bias of any device group
- Stable as long as gain blocks reduce currents
Complete Current Mirror

\[ \frac{I_{\text{OUT}}}{I_{\text{IN}}} \propto \frac{1}{N} \]

\[(N = 1 \ldots 4096)\]
Voltage-Controlled Oscillator

VCO Replica-Feedback Bias Generator

Buffer Stage

11-Stage Ring Oscillator
Buffer Tail Node Matching

\[ \Delta V \]

\[ \Delta I_L, \Delta I_H \]

\[ \Delta V \]

Higher \( V_{DD} \)

\[ V_{TAIL} \]

\[ V_{REP} \]
Modified VCO

VCO Replica-Feedback Bias Generator

Buffer Stage

11-Stage Ring Oscillator
Static Supply Sensitivity

![Graph showing frequency vs. V_{DD} for different supply voltage conditions. The graph compares the frequency response of 'SHORTED' and 'ORIGINAL' conditions.]
## PLL Implementation

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology</td>
<td>0.13µm N-well CMOS</td>
</tr>
<tr>
<td>Nominal Supply Voltage</td>
<td>1.5V (designed for 1.2V)</td>
</tr>
<tr>
<td>Total Occupied Area</td>
<td>0.38 x 0.48mm²</td>
</tr>
<tr>
<td>VCO Frequency Range</td>
<td>30 ~ 650 MHz</td>
</tr>
<tr>
<td>Multiplication Factor Range</td>
<td>N = 1 ~ 4096</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>7mW @ 240 MHz, 1.5V</td>
</tr>
</tbody>
</table>

![PLL Diagram](image)
Measured Jitter vs N (240MHz)
Conclusions

- Proposed PLL achieves wide N and F_{OUT} range

- PLL is self-biased with constant loop dynamics \( \left( \omega_N / \omega_{REF}, \zeta \right) \), independent of N, F_{OUT}, and PVT

- Sampled feed-forward network suppresses pattern jitter with effective \( \omega_C \) that tracks \( \omega_{REF} \)

- Achieves relatively constant period jitter of less than 1.7% as N is scaled from 1 to 4096