Ultra PLL

**Features**

- New state-of-the-art architecture using high-speed digital and analog circuits that offers unprecedented operating ranges and extremely high performance.
- Ultra low jitter performance for the most demanding SerDes and ADC reference clocks.
- Ultra wide frequency range with multiplication factors over 250,000 to support 32KHz to 1GHz references.
- Precise frequency control with a least 26 fractional bits (at least 10 precise) for extremely high fractional-N resolution.
- Optional spread spectrum support with programmable rate and depth to meet tight FCC requirements.
- Low power and compact size.
- Highly programmable so one PLL can be used for all applications on a SoC.
- TSMC, GLOBALFOUNDRIES and UMC processes from 65nm to 16nm.

**Specifications**

**Part No. TCI-TN28HPC-ULTRAPLL**

- Divided reference frequency range 15KHz - 1.08GHz
- /1 output frequency range 10MHz - 3.25GHz
- Reference divider values 1 - 256
- Integer feedback divider values ~1-262144 (1-2^18)
- Fractional feedback divider bits (min) 26 (10 precise)
- Output divider values 1-2048
- /1 output multiples of div. reference 1-262144
- Bandwidth adjustment ratio ~1:2^32
- Spreading depth adjustment range (typ) 0%-3%
- Spreading rate adjustment range (typ) 15KHz - 1MHz
- Feedback signal delay (max) n/a (FB Internal)
- Output duty cycle (nom, tol) 50%, +/-1%
- Static phase error (max) n/a
- Period jitter (P-P) (max) +/-1.5ps
- Long-term jitter (RMS) (max) <500fs (1MHz to Fout) (designed to meet industry standard reference clock specs.)
- Power dissipation (nom) 10mA
- Reset pulse width (min) 5us
- Reset /1 output frequency range ~3.25GHz if enabled
- Lock time (min allowed) 500 div. reference cycles
- /1 output freq. overshoot (max) 0%
- Area (including isolation) (max) ~0.035mm^2
- Number of PLL supply pkg. pins 1 VDDA, 1 VSSA (preferred)
- Low freq. supply noise est. (P-P) (max) +/-5% VDDA
- Low freq. sub. noise est. (P-P) (max) +/-5% VDDA
- Ref. input jitter (long-term, P-P) (max) 2% div. reference cycle
- Ref. input spread-spectrum modulation 3% (P-P)
- Reference H/L pulse width (min) 140ps
- Synchronous bypass included Yes
- Process technology TSMC CLN28HPC
- Supply voltage (VDDA) (nom, tol) 1.5V-1.8V, +/-10%
- Supply voltage (VDD) (nom, tol) 0.9V, +/-10%
- Junction temperature (nom, min, max) 70C, -40C, 125C
- GDSII and LVS Spice netlist, behavioral, synthesis and LEF models, and extensive user documentation.
- Integration support to ensure a successful tape out (included in standard design license fee).

**Deliverables**

- www.truecircuits.com/product_matrix.html